REMARKS

Claims 1 to 3 and 10 to 13 were pending in the present application. Applicant has amended claims 1 and 10 to 13. Claims 1 to 3 and 10 to 13 remain pending.

Rejections of Claims 1 to 3, 10, 12, and 13

The Examiner rejected claims 1 to 3, 10, 12, and 13 under 35 U.S.C. § 103(a) as being unpatentable over U.S. Patent No. 6,049,889 ("Steely, Jr. et al.") in view of U.S. Patent No. 5,850,556 ("Grivna").

Claim 1

Addressing Applicant's first argument, the Examiner stated:

> Given the broadest reasonable interpretation of the claim, the write command is a direct memory access (DMA) command because a DMA operation is performed at the receiving node after the data is transferred from the sending node to the receiving node as detailed by Steely in col. 7, lines 29 – 32. In other words, the above recitation of claim 1 requires a "command for writing a block of data from a local node to a remote node via one of the communication links". The "direct memory access (DMA)" in the recitation is just an adjective that modifies the "command" by describing a specific type of command. Thus, the "command" can be called a DMA command by one of ordinary skill in the art because it results in a DMA operation being performed.

February 9, 2006 Office Action, pp. 3 and 4. In view of Examiner's comments, Applicant has amended claim 1 to recite "a direct memory access (DMA) write command for performing an inter-node DMA transfer of a block of data from the local node to a remote node via one of the communication links." Thus, claim 1 now makes it clear that the DMA transfer occurs between nodes. Claim 1 now does not read on Steely, Jr. et al., which only discloses a local DMA transfer at a remote node.

Addressing Applicant's second argument, the Examiner stated:

> In this case the structure of Steely is perfectly capable of performing the intended use of "writing an entire line of memory from a local node to a remote node via the communication link when a new data is written into the line of memory even when the new data is smaller than the line of memory". For example, if an entire line of memory were written to the appropriate address space in the system of Steely, then that line of memory would be reflected to a remote node. Therefore the ability to reflect an entire line of memory is present in Steely, regardless of

> whether or not the written data is smaller than the line of memory. If data smaller than the line of memory were written, then surely the system of Steely would be able to reflect an entire line of memory. Since the system of Steely is capable of performing the function without a structural change, it meets the limitations.

February 9, 2006 Office Action, pp. 4 and 5. Applicant respectfully traverses.

Steely, Jr. et al. is totally silent as to performing this type of write. The Examiner cannot assume that Steely, Jr. et al. has the proper hardware and/or software to perform this type of write. Its hardware and/or software may be configured only to receive a write of an entire line of memory, at which time the entire line is reflected to another node. At most, the Examiner may assert that Steely, Jr. et al. can be modified to perform this type of write. However, the Examiner has yet to provide any detail as how Steely, Jr. et al. can be modified and what would be the motivation behind such a modification. Thus, the Examiner has yet to meet his burden for establishing a prima facie case for obviousness under §103(a).

Accordingly, amended claim 1 is patentable over the combination of Steely Jr. et al. and Grivna for the above reasons.

Claims 2, 3, and 10

Claims 2, 3, and 10 depend from amended claim 1 and are patentable over the cited references for at least the same reasons as amended claim 1.

Claim 12

The Examiner failed to address Applicant's previous argument regarding claim 12. Essentially, claim 12 recites "merging the new data with the existing data so the new data replaces some existing data while other existing data remains," which is not disclosed by Steely, Jr. et al. or Grivna. Claim 12 (emphasis added). This is not a parity calculation but a process to write an entire line of memory to a remote node with both old and new data when the new data is smaller than the entire line of memory. Accordingly, amended claim 12 is patentable over the combination of Steely, Jr. et al. and Grivna.

Claim 13

Rejecting claim 13, the Examiner stated that "Steely further teaches the communication link protocol of claim 12 above, wherein said writing a line of memory from a local node to a remote

node comprises the writing the line of memory to a remote node using a same address offset of the line of memory at the local node (col. 4, lines 16 – 21)." February 9, 2006 Office Action, p. 8. Applicant respectfully traverses.

Steely, Jr. et al. discloses that address translation is used to write data in local memory space of a sending node to a network address space, and then from the network address space back to a local memory space of a receiving node.

> For example, writes to the shared portion of memory address space 43 are translated by map 43a to an address in network address space. The network address is translated by map 44a in node 14 to an address of the node memory of node 14. Accordingly, node 12 communicates with node 14 via writes its own MC address space. Similarly, writes to the shared portion of memory address space 34 by node 14 are translated by map 44a to an address in network address space 33. The network address is translated by map 43a of node 12 into a node memory address for node 12. Such an arrangement allows for communication between the CPU or external I/O devices of node 12 and the CPU or external I/O device of node 14 by providing memory-mapped connections which are established between the nodes.

Steely, Jr. et al., col. 4, lines 16 to 29 (emphasis added). Thus, the lines of Steely, Jr. et al. cited by the Examiner actually support the Applicant's argument since they disclose address translation instead of using "same address offset" as recited in claim 13. Accordingly, claim 13 is patentable over the combination of Steely, Jr. et al. and Grivna.

Rejections of Claim 11

Addressing Applicant's argument, the Examiner stated:

> Steely teaches, "computing parity over multiple blocks of data from a local memory of the local node and writing the party to a remote memory of the remote node in a single operation." Steely states that parity from a local node is computed and written at the remote node in a single operation in col. 6, lines 37 – 39.

February 9, 2006 Office Action, p. 5. Applicant respectfully traverses.

Amended claim 11 now recites "wherein said performing an inter-node DMA transfer of a block of data from a local node to a remote node comprises computing parity over multiple blocks of data from a local memory of the local node and writing the parity to a remote memory of the remote

node in a single operation." Amended claim 11. Thus, the parity calculation is part of the inter-node DMA transfer.

Steely, Jr. et al. at col. 6, lines 37 -- 39 does not disclose an inter-node DMA transfer including such a parity computation and transfer. Instead, these cited lines disclose that data transmitted between nodes over a network bus 55 in a hub 21 has parity computed by state machines 50 and 52 in hub 21 as the data is transmitted at one end of the bus and as the data is received at another end of the bus. Accordingly, amended claim 11 is patentable over the combination of Steely, Jr. et al., Grivna, and Gunsaulus et al.

Summary

In summary, claims 1 to 3 and 10 to 13 were pending in the present application. Applicant has amended claims 1 and 10 to 13. Applicant requests the Examiner to withdraw his claim objections/rejections and allow claims 1 to 3 and 10 to 13. Should the Examiner have any questions, please call the undersigned at (408) 382-0480x206.

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Respectfully submitted,

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